

The Mark 5B VLBI Data System

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Abstract

The Mark 5B VLBI data system is designed to support the VSI-H international specification. It is based on the same physical platform and uses the same disk-modules as the Mark 5A; it also supports the same maximum data rate of 1024 Mbps. Data formatting and time-tagging is done internally within the Mark 5B. This allows, for example, existing VLBA systems to bypass the VLBA formatter, which is limited to 512 Mbps, and connect directly to the output of VLBA samplers (through a simple interface) at a maximum data rate of 1024 Mbps. For existing 14-BBC Mark IV systems, the Mark 5B allows connection of all 14 BBC's to two Mark 5B's for a total aggregate data rate of 1792 Mbps. In addition, the Mark 5B is designed to support all critical functionality of the Mark IV Station Unit, so that the Mark 5B may play back directly to the Mark IV correlator through a simple interface. The Mark 5B system is expected to be available to the VLBI community in early/mid 2006.

1. Mark 5B VLBI System Goals

Incorporating primarily low-cost PC-based components, the Mark 5B system [1] supports data rates up to 1024 Mbps, recording to an array of inexpensive removable IDE/ATA disks (see Figure 1). The general goals of the Mark 5B system are low cost, robust operation, 1 Gbps data rate, conformance to VSI-H specification, easy transportability, and 24-hour unattended operation at 1 Gbps.

All but the last goal have now been achieved; the last goal, 24-hour unattended operation at 1 Gbps, is expected to be attained by the end of 2006 with continued development in high-capacity disk technology.

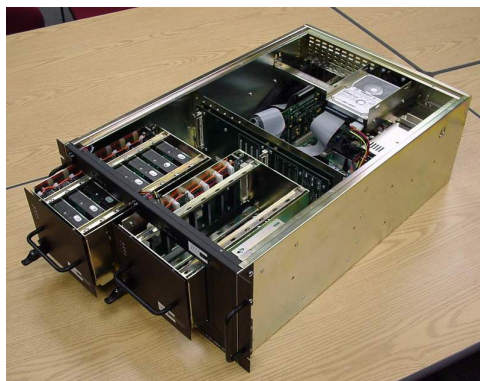


Figure 1. Mark 5 VLBI data system

2. Characteristics of the Mark 5B Data System

The Mark 5B system has the following characteristics:

- Uses the same chassis and disk packs as the Mark 5A (see Figure 1)
- Implements the VLBI Interface Standard
- Maximum record/playback data-rate is 1024 Mbps (same as Mark 5A)
- Requires new Mark 5B I/O card, currently under design
- Eliminates the need for an external formatter (but requires mating VSI interfaces)
- With a 14-BBC Mark IV DAS, up to 1792 Mbps can be recorded with two parallel Mark 5B systems
- Mark IV Station Unit capabilities are designed into the Mark 5B so that Mark 5B systems can be connected to Mark IV correlators without the use of a Mark IV Station Unit.
- Built-in phase-cal extraction and state-counting during recording and playback
- Xilinx FPGA design is updateable via software download from PC (Mark 5A FPGA requires programming from a separate external source)
- Upgrade from Mark 5A to Mark 5B requires only replacement of Mark 5A I/O interface card with a Mark 5B I/O interface card

3. Mark 5B Design

The Mark 5B can be configured as either a DIM (Data Input Module) or DOM (Data Output Module) via software control, which loads the selected personality into the on-board FPGA. We will describe the DIM and DOM separately.

3.1. Data Input Module (DIM)

The DIM is responsible for accepting the data on the VSI input connector, properly time-tagging it, and sending it to the Mark 5 disk module. A simplified block diagram of the DIM is shown in Figure 2.

DIM functionality is a straightforward implementation of the VSI-H specification [4]. 32 data bit-streams (BSn) accompanied by corresponding CLOCK, 1PPS and PVALID signals arrive on an MDR-80 connector carrying LVDS signals. The 1PPS signal is used just once (on command) to synchronize the internal Data Observe Time (DOT) clock, which thereafter keeps time only by counting CLOCK cycles. Two alternate external 1pps inputs are also available for synchronization, labeled ALT1PPS and ALT2PPS. ALT1PPS is carried on a VSI-specified MDR-14 connector with LVDS levels; ALT2PPS is available as a TTL-level SMB connector on the board. Only one of these 1pps signals may be selected to initialize the DOT clock. After DOT clock initialization, the external 1pps signal is not used by the DIM.

The number of active bit streams to be recorded may be 1, 2, 4, 8, 16 or 32, as per the VSI-H specification. The selected bit streams are multiplexed, as necessary, before writing to the 32-bit wide FPDP bus which drives the writing of the disks. The disk data are divided into sequential 10,000-byte Disk Frames (DF), each of which is preceded by a 32-byte non-data-replacement Disk

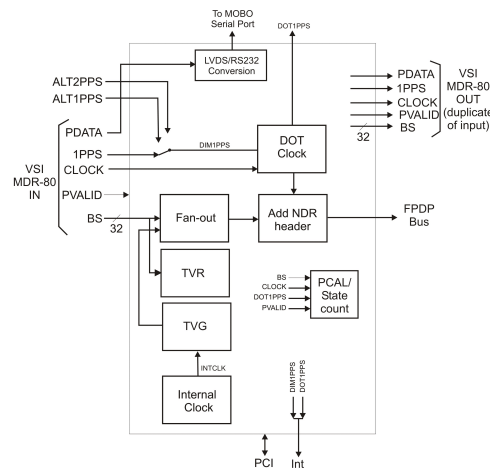


Figure 2. Simplified block diagram of Mark 5B DIM

Frame Header (DFH) and includes a sync-word, a DF number (modulo one second), and time encoded in the same format as a VLBA tape frame header, including the accompanying 16-bit CRCC code. The DF frame number is always reset to 0 at every second tick.

Also included in the DIM is a standard VSI test-vector generator (TVG) and test-vector receiver (TVR). The TVG data can be written to disk for analysis either by software, or may be played back to a TVR in a DOM.

An on-board phase-cal processor can extract 16 tones from each of 16 channels of data, as well as state counts for each channel [5]. Both the phase-cal and state-count information may be read every second; the state-count information may be used to dynamically adjust signal levels coming into the data-acquisition system in order to optimize the signal-to-noise ratio of 2 bit/sample data.

The PDATA signal is converted to RS-232 and sent to an on-board RS-232 connector, where it may be interfaced to a serial input port on the host PC for processing.

A ‘cascade’ mode of operation of the Mark 5B is supported so that the signals received on the VSI MDR-80 connector are replicated on a VSI MDR-80 output connector. This feature may be used to ‘daisy-chain’ Mark 5B systems together to extend the total unattended observing time.

3.2. Data Output Module (DOM)

The DOM is responsible for accepting data that has previously been recorded on disk, then reconstructing replicas of the original data streams and timing signals on the VSI MDR-80 output connector. A simplified block diagram of the DOM is shown in Figure 3.

When operating as a VSI DOM, operation is quite straightforward. External timing reference signals DPS1PPS and DPSCLOCK, normally generated by the correlator to which the DOM is interfaced, assure that the data output of the DOM is correct in epoch and rate. The data arriving from the disks via the FPDP bus are stripped of Disc Frame Headers, de-multiplexed as necessary, and a crossbar is used to restore the bit-streams to their original positions in the bit-stream mask. The data are then regenerated with a delay (w.r.t. the DPS1PPS and ROT1PPS ticks) according to user specification. The signals emerging from the VSI output MDR-80 connector are a mirror of the signals which were input into the DIM at the time of the recording. An on-board phase-cal

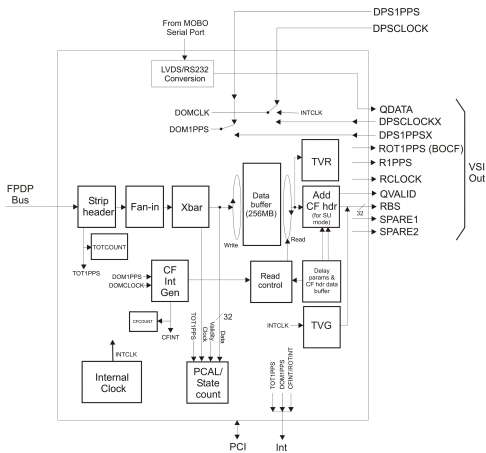


Figure 3. Simplified block diagram of Mark 5B DOM

processor can extract 16 tones from each of 16 channels of data, as well as state counts for each channel; the processing results are read periodically and transmitted to the correlator.

The DOM also includes both a TVG and a TVR for testing purposes.

4. Station Unit Emulation Capability

Configured as a DOM, the Mark 5B can also act as a replacement for the Mark IV Station Unit so that the Mark 5B can interface directly to a Mark IV correlator. Operating in DOM station-unit mode, the Mark 5B has several functions:

- Delays the data according to a fifth-order spline polynomial supplied to the Station Unit before presentation to the correlator proper
- Inserts headers into the data stream with model information to be used by the correlator proper
- Extracts up to 16 phase-calibration signals from each channel
- Counts state statistics to properly normalize correlation coefficients

The implementation of these functions is aided by an on-board 256 MB memory module which allows rapid dynamic changes in the data-delay at intervals specified by the controlling delay model.

5. Mark 5B I/O Interface Board

An annotated photo of the Mark 5B I/O board [6] is shown in Figure 4. Note that there are separate MDR-80 connectors for VSI-H input and output. Also note the 256MB memory module that is piggybacked onto the board to support operation of the Mark 5B in ‘station unit’ mode.

6. Playback Compatibility with Mark 5A

The Mark 5B data format is designed so that disk modules recorded on a Mark 5B in several commonly-used modes can be played back on an enhanced Mark 5A unit, dubbed ‘Mark 5A+’.

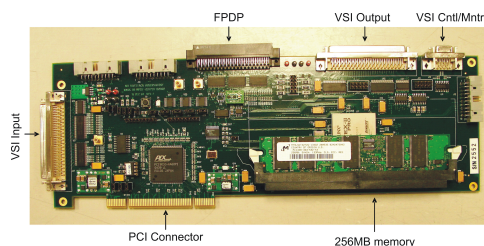


Figure 4. Mark 5B I/O Interface Board

The Mark 5A+ requires that additional capability be added to the Mark 5A; the engineering work to add this capability is now in progress and will require only a reconfiguration of the FPGA on the Mark 5A I/O interface board. The playback format of the Mark 5A+ unit when reading Mark 5B disks will be VLBA track format. This ‘compatibility’ mode will allow data recorded on Mark 5B systems to be correlated on existing Mark 5A correlators during the transition period to Mark 5B.

7. Summary

The Mark 5B system is the second in the line of Mark 5 VLBI data systems and the first to implement the VSI-H standard. Built on the same platform as the Mark 5A, the Mark 5B offers both a simple migration path for existing Mark 5A users and an inexpensive VSI-compatible VLBI data system for new installations. In addition, a Mark 5B/Mark 5A compatibility path has been established to ease in the transition from Mark 5A to Mark 5B. The Mark 5 systems are being developed with support from BKG, JPL, KVN, MPI, NASA, JIVE, NRAO and USNO. When development is completed, the Mark 5B system design will be transferred to Conduant Corporation in Longmont, CO for replication and distribution to the VLBI community.

References

- [1] The Mark 5 web site at <http://web.haystack.mit.edu/mark5/Mark5.htm> contains much additional information about the Mark 5 system.
- [2] “VLBI Standard Hardware Interface Specification - VSI-H”, Revision 1.0, 7 August 2000, available at <http://dopey.haystack.edu/vsi/index.html>.
- [3] “Mark 5B design specifications”, available at <ftp://web.haystack.edu/pub/mark5/019.pdf>.
- [4] “Data Input Module Mark 5B I/O Board Theory of Operation”, available at <ftp://web.haystack.edu/pub/mark5/032.pdf>.
- [5] “Phase Cal Extraction for the Mark 5B”, available at <ftp://web.haystack.edu/pub/mark5/021.pdf>.
- [6] “Mark 5B I/O Board Physical Description”, available at <ftp://web.haystack.edu/pub/mark5/031.pdf>